POWER SUPPLY PROCESSING FOR
POWER AMPLIFIERS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to power supply processing for power amplifiers.

2. State of the Art

High-efficiency power amplifiers (PAs), including radio frequency (RF) power amplifiers of a type used in RF transmitters, may be based on switch-mode techniques in which a transistor of a final amplification stage is driven between two states, a hard-on state and a hard-off state. In switch-mode operation, the output power of the final amplification stage is determined primarily by the power supply to the final amplification stage. In order to perform output power control, therefore, a mechanism is required to vary the power supply to the final amplification stage. One representative patent describing switch-mode PA techniques and corresponding power supply processing techniques is U.S. Patent 3,900,823 entitled AMPLIFYING AND PROCESSING APPARATUS FOR MODULATED CARRIER SIGNALS, issued August 19, 1975, incorporated herein by reference.

Three principle issues are raised with regard to power supply processing. One issue is the speed with which the power supply can be varied. Another issue is efficiency, or the extent to which losses incurred in power supply processing can be minimized. A final issue is circuit complexity and cost. Ideally, a simple, inexpensive power converter would enable rapid and precise changes in power supply. In practice, this ideal has proved unattainable. Further improvement is needed in order to achieve efficient, low-cost power amplifiers

SUMMARY OF THE INVENTION

The present invention, generally speaking, uses multiple selectable power supply paths, a saturation detector, or combinations of the same to achieve effi-

cient power supply processing. In one aspect of the invention, a power supply processing circuit includes a first switched converter stage and a second linear stage. Depending on the power supply desired, the first stage may be bypassed to avoid conversion losses. In another aspect of the invention, a saturation detector is used to control the first stage such that the second stage operates efficiently just short of saturation, thereby avoiding distortion.

BRIEF DESCRIPTION OF THE DRAWING

The present invention may be further understood from the following description in conjunction with the appended drawing. In the drawing:

Figure 1 is a diagram of a saturation prevention circuit that may be used with an exemplary embodiment of the invention;

Figure 2 shows one particular implementation of the saturation detector of Figure 1;

Figure 3 is a diagram of an RF amplifier with which the saturation detector may be used;

Figure 4 is a diagram of an alternative saturation prevention circuit;

Figure 5 is a block diagram of a power supply processing arrangement in accordance with one aspect of the present invention;

Figure 6 is a block diagram of another power supply processing arrangement;

Figure 7 is a block diagram of a further power supply processing arrangement;

Figure 8 is a block diagram of yet another power supply processing arrangement; and

Figure 9 is a plot illustrating, for switch mode power supplies of different assumed efficiencies, a threshold point at powers above which bypassing of the switch mode power supply is advantageous.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention is applicable to power amplifiers of all types, includ-

ing switch mode power amplifiers, linear power amplifiers, etc. Therefore, although the following illustrative embodiments pertain especially to switch mode power amplifiers, it should be recognized that various other embodiments are equally embraced by the present disclosure. Referring now to Figure 1, a diagram is shown of a saturation prevention circuit that may be used with an exemplary embodiment of the invention. (The saturation prevention circuit itself is the subject of U.S. Patent Application _____, entitled SATURATION PREVENTION AND AMPLIFIER DISTORTION REDUCTION, filed December 15, 2000 and incorporated herein by reference.) A transistor Q1 is coupled to a power source, Vbat, and to a load L.

In the present application, the load L is an RF amplifier as illustrated in Figure 3 and described in greater detail in U.S. Patent Application 09/247,095, entitled HIGH-EFFICIENCY MODULATING AMPLIFIER, filed February 9, 1999 and incorporated herein by reference. Briefly, the amplifier is part of a polar (as opposed to I-Q) amplifier architecture in which separate amplitude and phase paths are provided. The phase path is coupled to an RF input of the amplifier. The amplitude path is coupled to the power supply input of the amplifier. In the embodiment of Figure 3, therefore, circuitry 300 functions as an AM modulator.

Referring again to Figure 1, in this configuration, the transistor Q1 is a bipolar transistor having an emitter terminal coupled to Vbat and a collector terminal coupled to the load L. The collector terminal is also coupled to a resistive network comprising series-connected resistors R1 and R2 coupled to ground. A voltage occurring at node A between the resistors R1 and R2 is proportional to the voltage applied to the load L. A resistor R3 is coupled between the emitter terminal and the base terminal of the transistor Q1. The combination of the resistors R1-R3 allows the gain of the transistor Q1 to be set.

An operational amplifier (op amp) 101 is provided as part of a feedback circuit used to control the transistor Q1 and thus set a voltage applied to the load L.

(The operational amplifier may be in either discrete or integrated form.) A positive input terminal of the op amp is connected to node A of the circuit. In concept, the negative input terminal is coupled to a command input signal 103, and an output signal of the op amp 101 is coupled to the base terminal of the transistor Q1. In the illustrated circuit, however, a current monitor 105 is inserted between the output signal of the op amp 101 and the base terminal of the transistor Q1.

Furthermore, since in the illustrated circuit the command input signal is digital and the op amp 101 requires an analog input signal, a digital-to-analog converter (DAC) 107 is inserted in this path. The DAC 107 is a multiplying DAC, allowing a scale factor to be applied to the command input signal. The scale factor to be applied (at least in the absence of saturation) is stored in a multiplier register 108. This value determines the power output to the load.

Saturation prevention is carried out in response to the current monitor 105, by a threshold comparator 109 and modification logic 111. The threshold comparator is coupled to the current monitor 105 and to the modification logic 111. The modification logic is coupled to the threshold comparator 109, the multiplier register 108, and the DAC 107. Together, the modification logic 111, multiplier register 108 and multiplying DAC 107 perform a scaling function represented by block 120.

Operation of the saturation prevention circuit is based on the following principle. In order to achieve a particular voltage at node A of the circuit, the required base current into the transistor Q1 will varying linearly with the desired voltage throughout the linear range of the transistor Q1. However, as the transistor Q1 approaches saturation, the base current will rapidly rise (by action of the feedback arrangement) in an unsuccessful attempt to raise the voltage at node A to the desired level. This rapid rise in base current is detected immediately by the current monitor 105 in combination with the threshold comparator 109. The onset of saturation is thus signalled to the modification logic 111. The modification logic then

modifies downward the scale factor stored in the multiplier register such that an appropriately reduced scale factor is applied to the multiplying DAC 107. As a result, the transistor Q is driven less heavily, and saturation is rapidly averted.

The modification logic may vary from simple to complex, and may be implemented in hardware or as code executed by a processor (as in U.S. Patent 5,021,753, for example).

Referring to Figure 2, one particular implementation is shown, illustrating further details of the current monitor 105 and the threshold comparator 109. The current monitor may take the form of an emitter-follower stage comprising a transistor Q2 and resistors R4 and R5. The threshold comparator may take the form of a common-emitter stage comprising a transistor Q3 and resistors R6 and R7. In operation, a current flows through the resistor R4 that is proportional to the base current of the transistor Q1, and a related current flows through the resistor R7. Depending on that magnitude of the latter current, the output voltage developed at the comparator output will be either below or above a logic threshold of the scaling circuit 120.

The foregoing principle of saturation detection is applicable to various different types of active elements, including, for example, field-effect transistors (FETs). An example of such a circuit is shown in Figure 4, in which the transistor Q1 of Figure 1 has been replaced by a FET M1. The current monitor 105 and the resistor R3 are omitted from the circuit of Figure 4. In addition, the threshold comparator of Figure 1 is replaced by a voltage comparator 309. As the transistor M1 approaches saturation, the gate voltage will rapidly drop (by action of the feedback arrangement) in an unsuccessful attempt to raise the voltage at node A to the desired level. This rapid drop in gate voltage is detected immediately by the voltage comparator 309 to enable corrective action to be taken.

The above descriptions apply to p-type output transistors. Similar circuits may be used with n-type output transistors (e.g., NPN, NMOS, etc.).

Referring now to Figure 5, a block diagram is shown of a power supply processing arrangement in accordance with one aspect of the present invention. An RF power amplifier is provided, constructed in accordance with a polar architecture having a phase path and a separate amplitude path. In the phase path, a phase modulator 503 receives a phase modulation signal and a carrier signal and produces a phase modulated carrier signal, which is applied to the RF input of a switch-mode power amplifier (SMPA) 505. The SMPA may include multiple amplifier stages. In the amplitude path, an amplitude modulator 507 receives an envelope modulation signal and produces an envelope voltage, Venv (which may be a single voltage signal or multiple different voltage signals for multiple different amplifier stages). The envelope voltage is applied to the power supply input(s) of the SMPA.

In the arrangement of Figure 3, described previously, the amplitude modulator 300 receives the main power supply voltage directly. In such an arrangement, when a large voltage difference exists between the main supply and the desired envelope voltage signal, this voltage difference is dropped across the amplitude modulator, resulting in inefficient operation.

Referring again to Figure 5, this inefficiency is avoided (as also described in the second aforementioned co-pending application) by providing a switch-mode power supply (SMPS) 509 coupled between the amplitude modulator and the main supply. The envelope modulation signal is applied to control logic 511 (also powered from the main supply), which produces a control signal Vin for the SMPS. In response, the SMPS produces a voltage V_{SMPS} that is some small voltage ΔV greater than the desired voltage Venv. The small voltage ΔV allows for a voltage drop across the active device of the amplitude modulator and is no greater than required to keep the device in its active region.

Further improvement may be obtained using the foregoing saturation detector, incorporated in the form of saturation detector 513 as part of the ampli-

tude modulator 507. A saturation detection signal AM SAT is applied to the control logic. In response, the control logic boosts the command signal Vin by increasing ΔV incrementally until the saturation detection signal ceases.

For long-term efficiency, it is desirable to minimize ΔV. For this purpose, the control logic may be programmed to, either continuously or periodically, reduce ΔV incrementally until saturation is detected. Various control programs may be devised to achieve this manner of operation. Basically, if saturation is detected too frequently, excessive signal distortion may result. If saturation is detected too infrequently, unnecessary power dissipation may result.

In some situations -- for example if the envelope signal is not accessible -- it may be desirable for the control logic to operate independently, without envelope information. (Accordingly, the envelope signal input to the control logic is indicated in dashed lines in Figure 5.) In this mode of operation, the following procedure may be performed, at the Nyquist rate relative to the envelope signal:

1. Lower the SMPS control signal Vin until the saturation detection signal occurs.

2. Change Vin to cause the SMPS to raise the output of the SMPS by some nominal amount (e.g., 100mV).

Bypassing the SMPS

The efficiency of the SMPS will typically be in the range of 80-90%. However, as illustrated in Figure 9, it has been found that at high output power (when Venv is near the main supply voltage), greater efficiency may be achieved by bypassing the SMPS. The power supply processing arrangement of Figure 5 may therefore be modified as shown in Figure 6. In Figure 6, the power amplifier 601 has been shown in greater detail as including three stages, the power supply inputs of the first two stages being commonly controlled and the power supply input of the third (final) stage being controlled separately. Note, however, that such an arrangement is illustrative only and not required for purposes of the present inven-

tion. An RF input signal to the first stage is produced by a phase modulator 603, controlled by a control circuit 611.

As in the previous-described arrangement, a SMPS, or DC/DC converter 609, is interposed between a transistor Q3 and the main supply, Vbattery. The transistor Q3 functions as an AM modulator, producing the voltage Venv applied to the power supply input of the final stage.

In this embodiment, the DC/DC converter is assumed to not be envelope-following. Therefore, the DC/DC converter is controlled from an AM/power control block 615 by a signal PCO that performs power control only. The transistor Q3 is controlled from the same block by a signal MOD that performs modulation control only. At power levels below some threshold, the voltage Venv is produced through the following path: from the supply, through the DC/DC converter, and through the transistor Q3.

In addition, a further path is provided, in parallel to the foregoing path, by a transistor Q1 coupled between the supply and the power supply input of the final stage. The transistor Q1 is controlled from the AM/power control block by a signal MPC that performs both modulation and power control. At power levels above the threshold, this path is the active path, and the transistor Q3 is cut off, disconnecting the DC/DC converter from the rest of the circuit.

In both low-power and high-power modes, stages 1 and 2 of the power amplifier are powered through a transistor Q2, controlled by the control circuit. The transistor Q2 may be coupled directly to the supply or may be coupled to the output of the DC/DC converter (or, possibly, an additional DC/DC converter). The power supply to these stages 1 and 2 may be held at a constant voltage Vk, or may be varied to perform additional power control and/or efficiency enhancement.

The AM/power control block may be provided with the saturation detector (indicated in dashed lines) described previously and may incorporate the same or similar control strategies as described previously.

A further embodiment is shown in Figure 7. In this embodiment, the DC/DC converter is assumed to be envelope-following. Therefore, the control signals from the AM/power control block both perform both power control and modulation and are therefore designated MPC1, MPC2 and MPC3.

Still a further embodiment is shown in Figure 8. In this embodiment, multiple power supply branches are provided, each including a transistor and all but one including a fixed DC/DC converter. At any given time, a single one of the power supply branches is active, depending on the desired output power level. In the case of the other branches, their transistors are cut off. Advantageously, the DC/DC converters may take the form of switch capacitor power supplies (known per se) which are fixed at fractional voltages of the battery voltage. This realization avoids large inductors that would otherwise be required in typical switch mode power supply implementations.

Thus there have been described power supply processing arrangements using multiple selectable power supply paths, a saturation detector, or combinations of the same to achieve efficient power supply processing. Using these arrangements, high efficiency and low distortion may be achieved simultaneously.

It will be appreciated by those of ordinary skill in the art that the invention can be embodied in other specific forms without departing from the spirit or essential character thereof. The presently disclosed embodiments are therefore considered in all respects to be illustrative and not restrictive. The scope of the invention is indicated by the appended claims rather than the foregoing description, and all changes which come within the meaning and range of equivalents thereof are intended to be embraced therein.